8.3 Low-Voltage-Swing Logic Circuits for a 7GHz X86 Integer Core

Daniel J. Deleganes, Micah Barany, George Geannopoulos, Kurt Kreitzer, Anant P. Singh, Sapumal Wijeratne

Intel, Hillsboro, OR

Pentium® 4 processor architecture uses a 2x frequency core clock[1] to implement low latency integer ops. Low-voltage-swing logic circuits implemented in 90nm technology[2] meet the frequency demands of a third generation integer-core design.

Figure 8.3.1 shows the chosen LVS circuit topology [4]. Inverters drive complementary data into a dual rail N-channel diffusion connected network (DCN). The DCN is reset low and equalized. During small signal development, one side evaluates high with transistors operating primarily in the linear region. The higher N-channel linear region current compared to P makes this the system of choice. The DCN gates are driven by either static or domino circuits. The first logic level control is always qualified with DCN reset, to avoid contention.

The DCN ends in a high-speed low-gain ratio'd P-type sense amplifier feeding a final high-gain stage implemented as a cross-coupled domino logic (CDL) gate (Fig. 8.3.2). Together these stages amplify 10% VCC differential (average) to full rail outputs. The DCN logic function signal development is allocated less than 35% of a 2x clock phase, equivalent to 2 nominal inverter delays; during this time it implements up to 6 effective logic stages. The gain stages cost less than two stage delays.

Figure 8.3.3 shows the timing sequence. The DCN reset killing differential immediately after the sense amp trigger is the only functional race.

As shown in Fig. 8.3.3, the non-zero offset level on the sense amp '0 output induces a glitch on the non-switching CDL output mitigated by the CDL's cross-coupled P-keepers. Below a minimum input differential, the glitch induces a domino false-discharge failure on the CDL output. This glitch magnitude is a criterion used by an in-house LVS timing and noise tool (LVSTNT) to calculate the circuit setup time. A second criteria is a minimum input differential, typically 8-10% of supply, needed to overcome noise, sense amp V-offset and process variation.

LVSTNT uses a patented pruning algorithm [3] to exhaustively search all circuit paths constrained by logic equations embedded as schematic properties; RTL codes equivalent equations that are formally verified against the schematic versions. As an illustration, the rotator/shifter described later exceeds 42,000 paths for verification. Including all differential noise scenarios increases the path count 10X.

Matching analog layout rules are required in 3 dimensions up to the layer above the last metal used for small signal interconnect. An in-house analog layout rule checker is built to enforce adherence to matching rules. In this way, essentially random logic is proven, by post layout extraction tools, to have minimal differential noise.

LVS technology enables a non-traditional implementation of the L0 data alignment mux. The circuit topology includes 128 individual 32 to 1 dual rail muxes. This function is accomplished in a single stage of logic by distributing the 'mux' node over the height of the L0. The large capacitance of the mux node and the large resistance of the distributed network results in small signal that is amplified to rail by the two gain stages described previously. Duplicating and distributing the mux reset and select logic along the height of the block ensures signal integrity. This single stage alignment mux operating in less than one 2x clock phase reduced the critical load pipeline in the integer core.

The LVS carry chain for a 16b adder is shown in Fig. 8.3.4. It is built upon 16-cascaded LVS PGK cells "0-F" with carry-skip pass-gates "S0-S9" positioned such that any carry propagation path traverses through no more than 6 series devices. The LVS cells that make up the LVS carry-chain are basic pass gate logic configurations with generate and kill transistors at each bit position. The LVS XOR gates hookup to each polarity of the carry[n] nodes along the chain to produce the sum [n+1] result. The typical critical path begins with the turning ON of the "s0" skip pass-gate that allows the "Cin" to charge up the reset-low carry-chain and develop differential at the inputs of 17 PMOS sense-amplifiers that sense the 16 sum and final carry results along this structure.

The carry propagation RC delays for a 32b LVS adder are too slow to sustain the frequency targets of the integer core. For this reason all IA32 ALU and AGU adders are built upon a common 16b LVS adder core. The 32b ALU for example employs 3 of these cores in a carry-select configuration. This common core is allocated only one 2x clock phase to compute a 16b add. Thus the add portion of the AGU and ALU operations on Si are operating at 2x the quoted frequency of the integer core. Fast P-interrupt ratio'd NOR gates are employed to generate the controls for the carry-skip pass-gates that initiate the carry propagation critical paths through the LVS adder.

A fast rotator/shifter performs fast latency shift and rotate ops. The circuit topology for the rotator/shifter data path is shown in Fig. 8.3.5. The two main components are the front-end circuits, and the rotator/shift logic.

The front-end forms the interface between single-ended full-swing input buses and dual-rail LVS logic. Similar "front end" muxes are found in all LVS structures attached to the result busses. Note the clocked "Thru Gate" which decouples the operand busses from the DCN during DCN reset.

Rotate ops are performed by steering the operand through a series of LVS muxes whose selects are calculated from the shift count. In parallel, LVS shift count logic determines bit by bit whether to select the rotated operand value or the "kill value". The kill value is always '0 for SHL and SHR ops, and is the size-appropriate most-significant bit for SAR ops.

The described LVS integer core is fabricated on 90nm technology. The processor includes test hardware that isolates the integer core on Si. Figure 8.3.6 shows the isolated core's voltage versus frequency schmoo running all tests. The LVS integer core exceeds 7.0 GHz on initial Si at 70C case/1.35V device and is expected to scale over time with process and post-Si optimizations. As a perspective, the count of non-array physical transistors involved, 6.8 million, exceeds the original Pentium® III microprocessor.

References

[1] D. Sager et al., "A 0.18μm CMOS IA32 Microprocessor with a 4GHZ Integer Execution Unit," *ISSCC Dig. Tech. Papers,* pp. 324-325, Feb. 2001.
[2] S. Thompson et al., "A 90nm Technology Featuring 50nm Strained Silicon Channel Transistors, 7 Layers of Cu Interconnects, Low k ILD, and 1μm² SRAM Cell," 2002 *IEDM Digest,* pp. 61-64, Dec. 2002.
[3] K. Stevens and M. Morrise, "Algorithm for Finding Vectors to Stimulate All Paths and Arcs Through an LVS Gate," *U.S.Patent 6557149*
[4] T. Sakurai et al., "Low-Power CMOS Design through Vth Control and Low-Swing Circuits," *Int. Symp. Low Power Electronics and Design*, pp. 1-6, Aug. 1997

 0-7803-8267-6/04

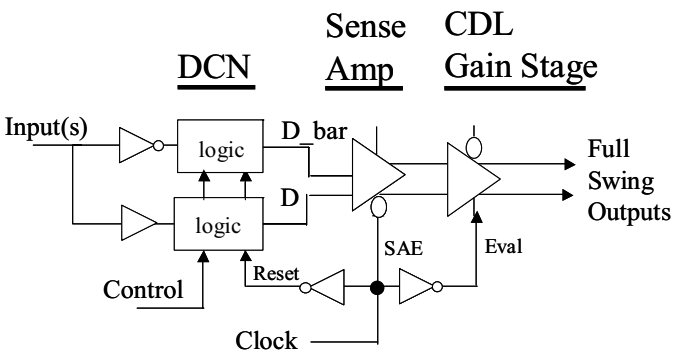

Figure: 8.3.1: Basic LVS topology used.

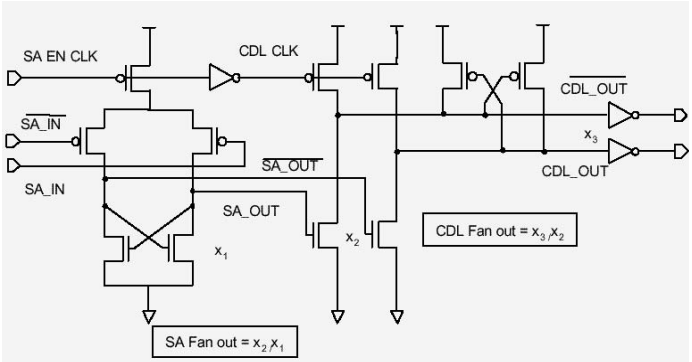

Figure: 8.3.2: Sense amp and CDL gain stage.

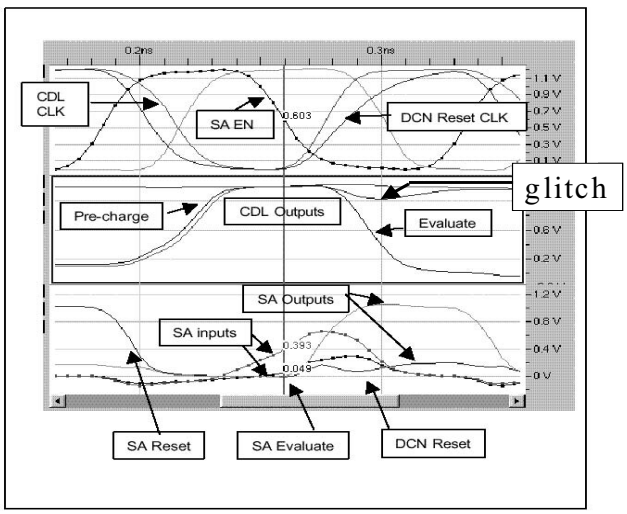

Figure: 8.3.3: LVS system timing sequence.

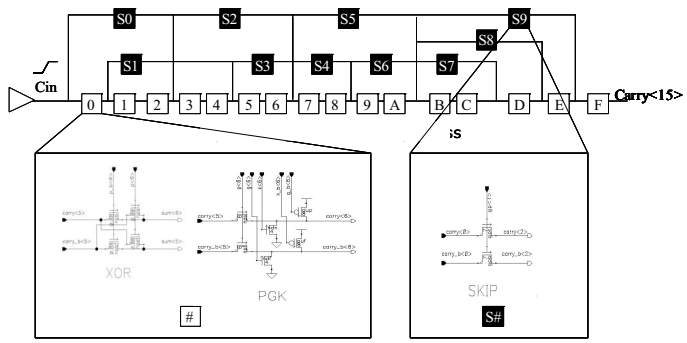

Figure: 8.3.4: LVS adder carry skip chain.

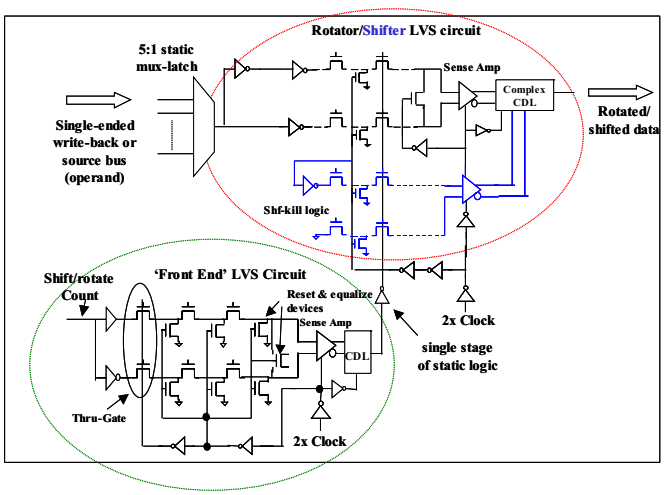

Figure: 8.3.5: LVS rotator/shifter topology.

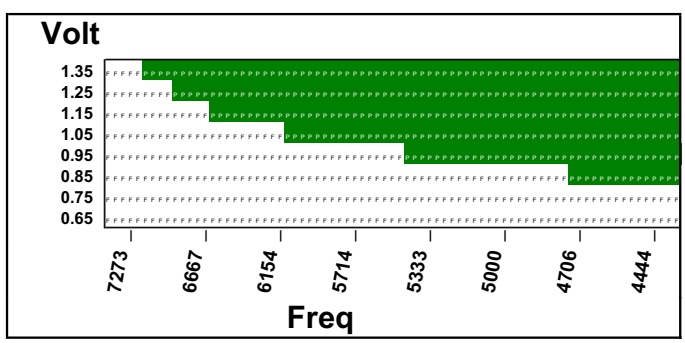

Figure: 8.3.6: LVS 2X clock integer frequency data.

0-7803-8267-6/04

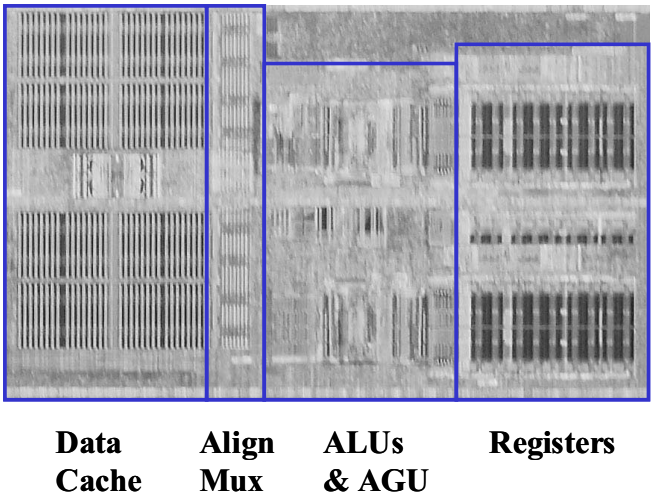

Figure 8.3.7: Integer core micrograph.

0-7803-8267-6/04

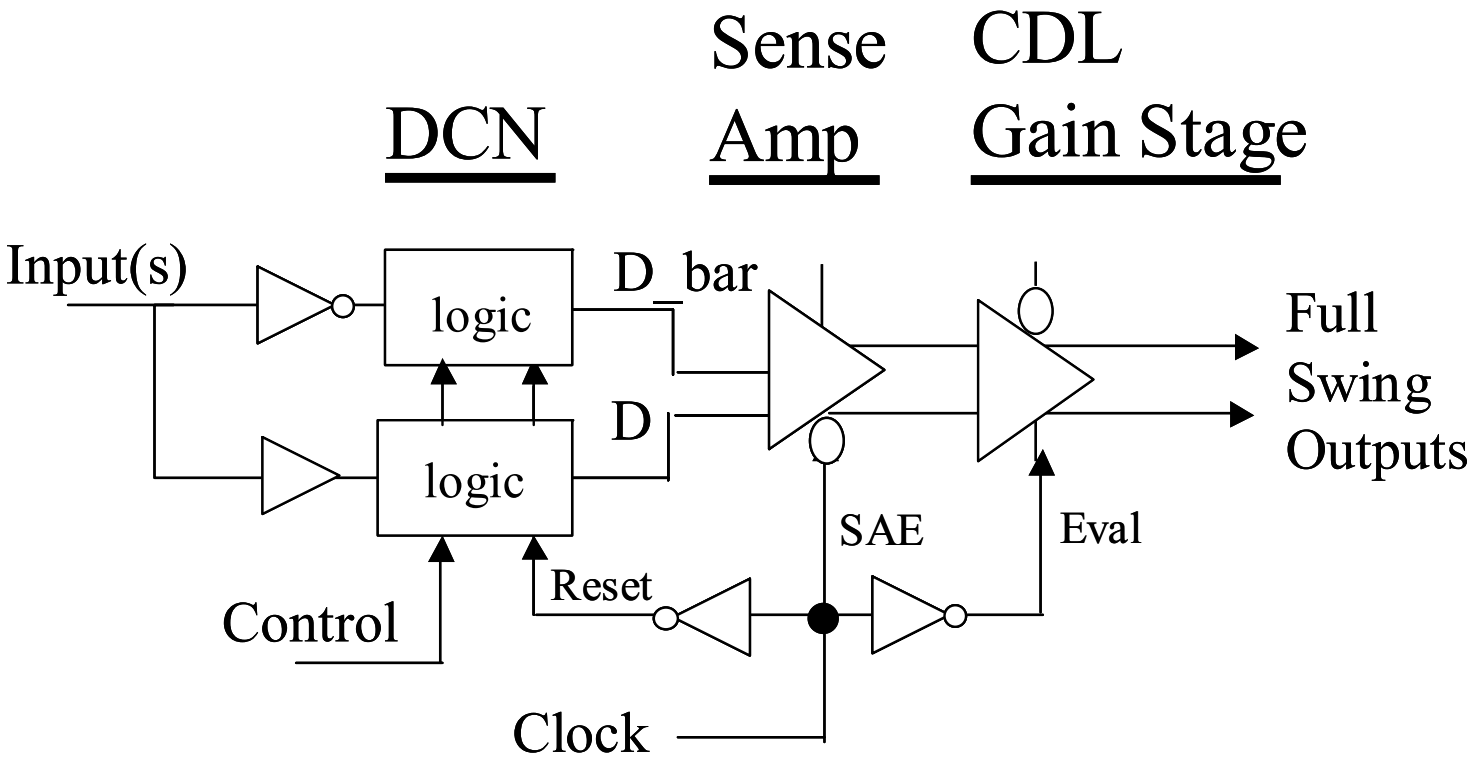

Figure: 8.3.1: Basic LVS topology used.

0-7803-8267-6/04

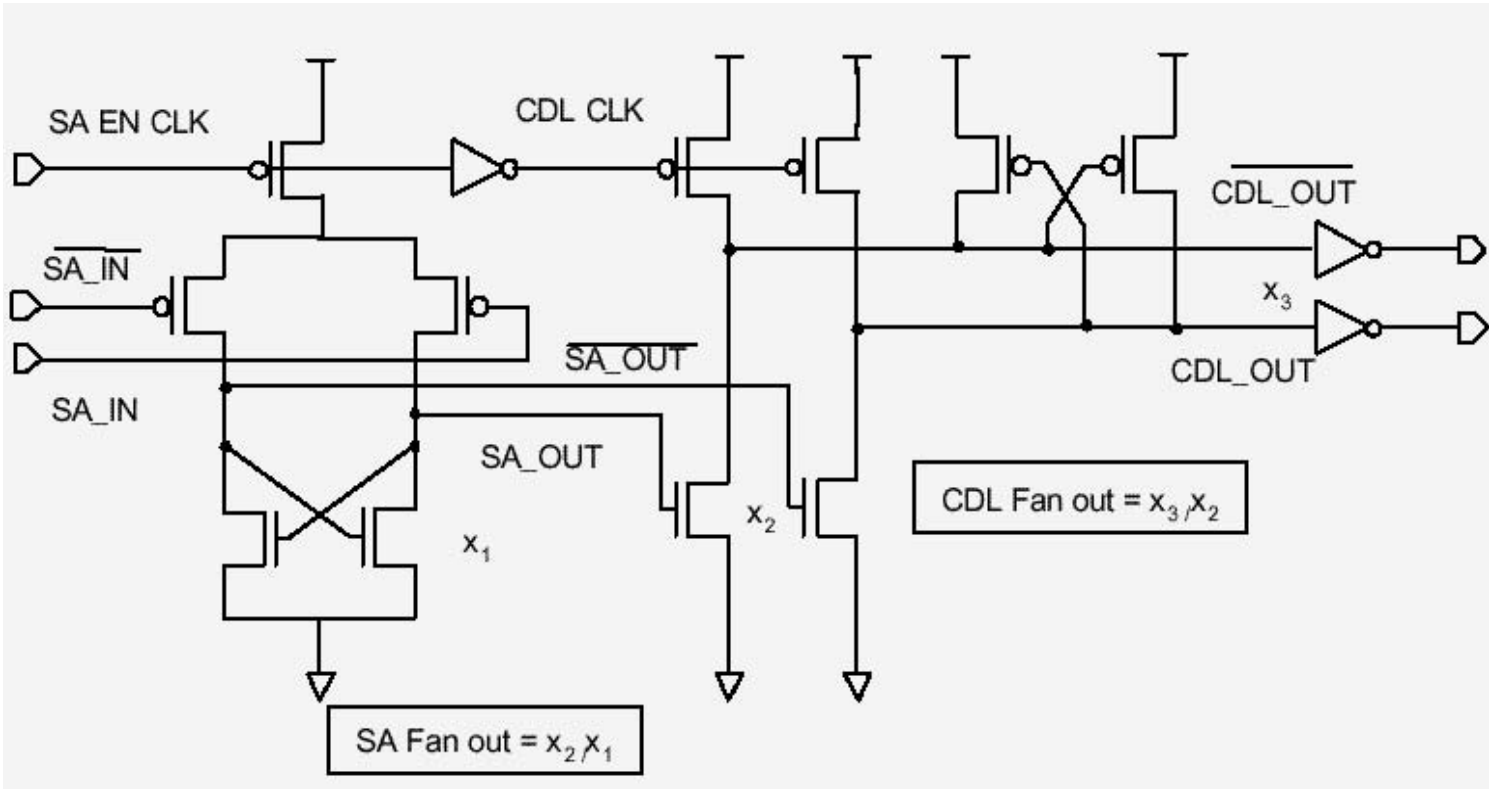

Figure: 8.3.2: Sense amp and CDL gain stage.

0-7803-8267-6/04

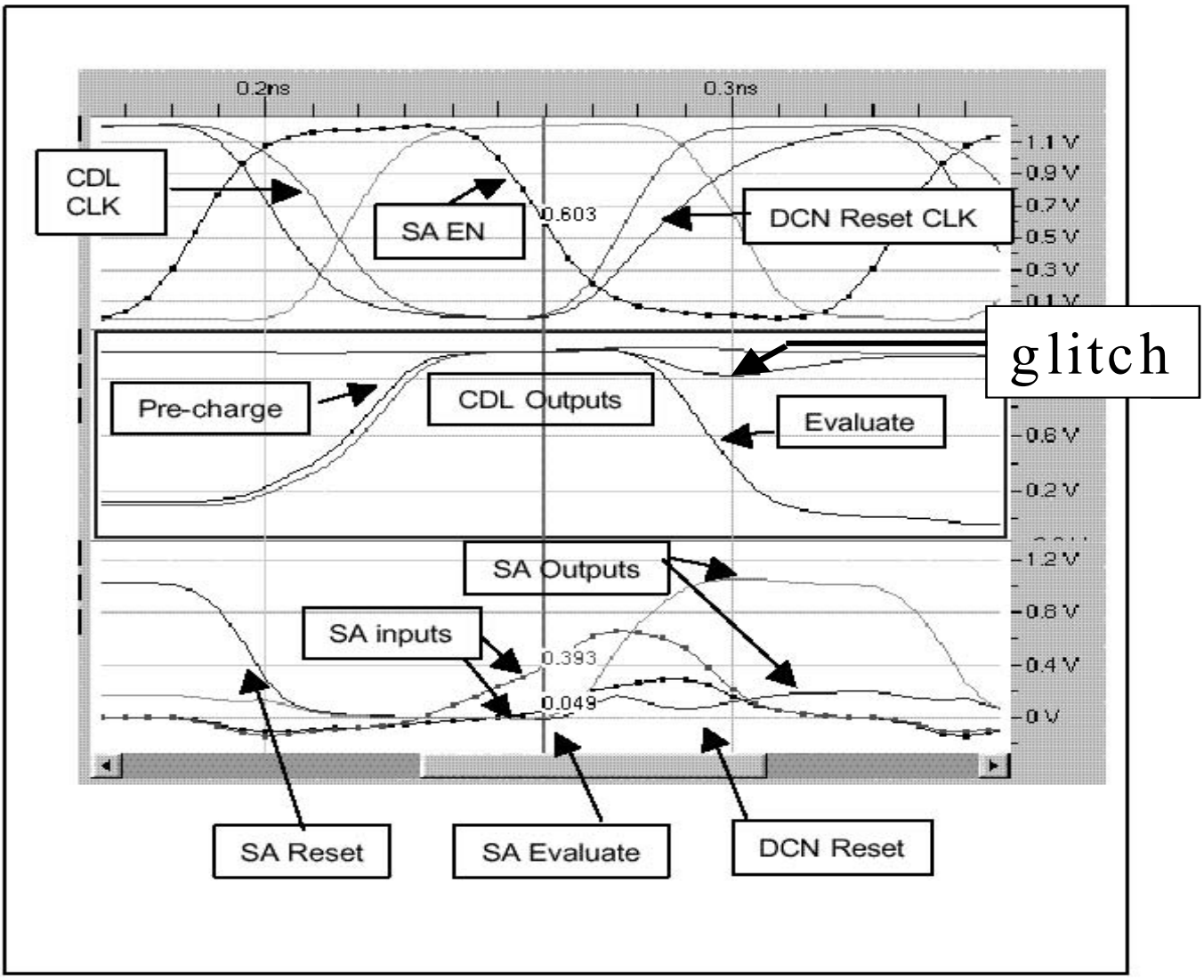

Figure: 8.3.3: LVS system timing sequence.

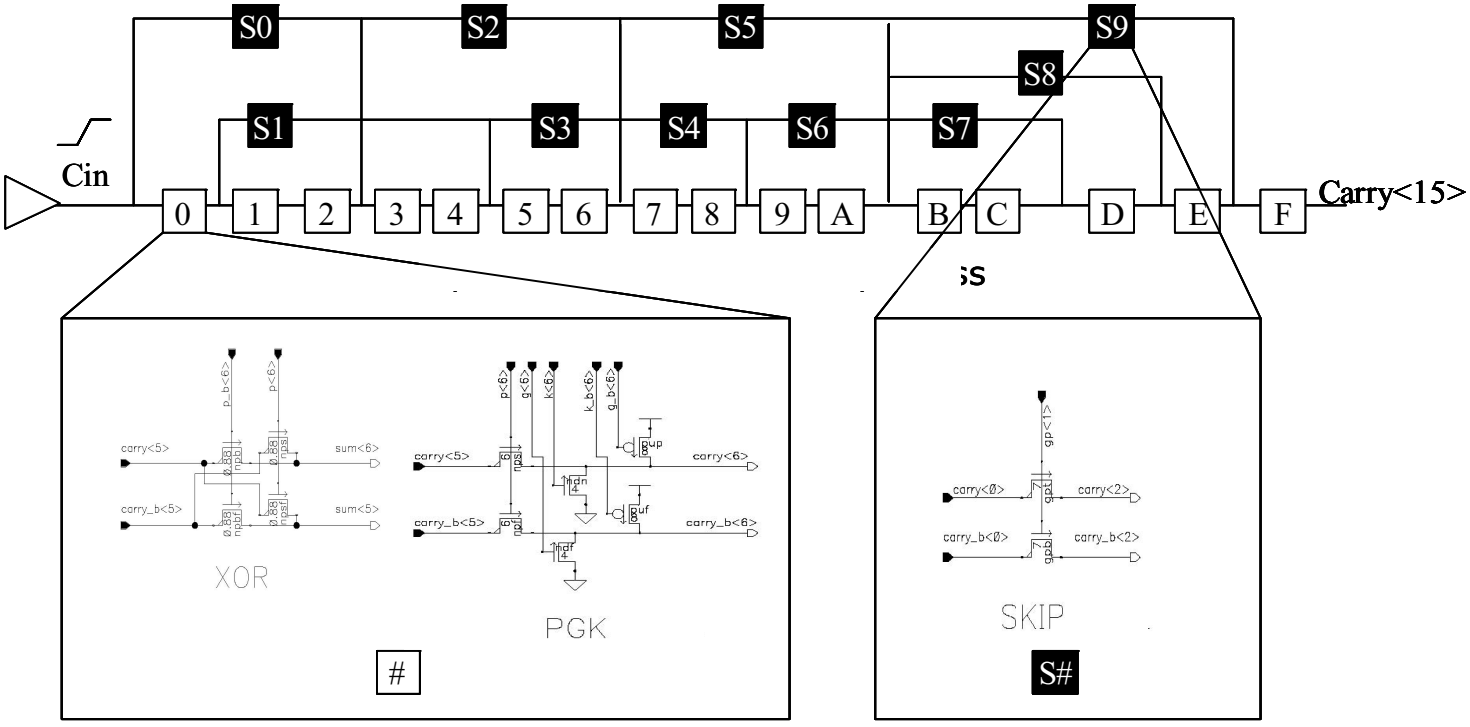

Figure: 8.3.4: LVS adder carry skip chain.

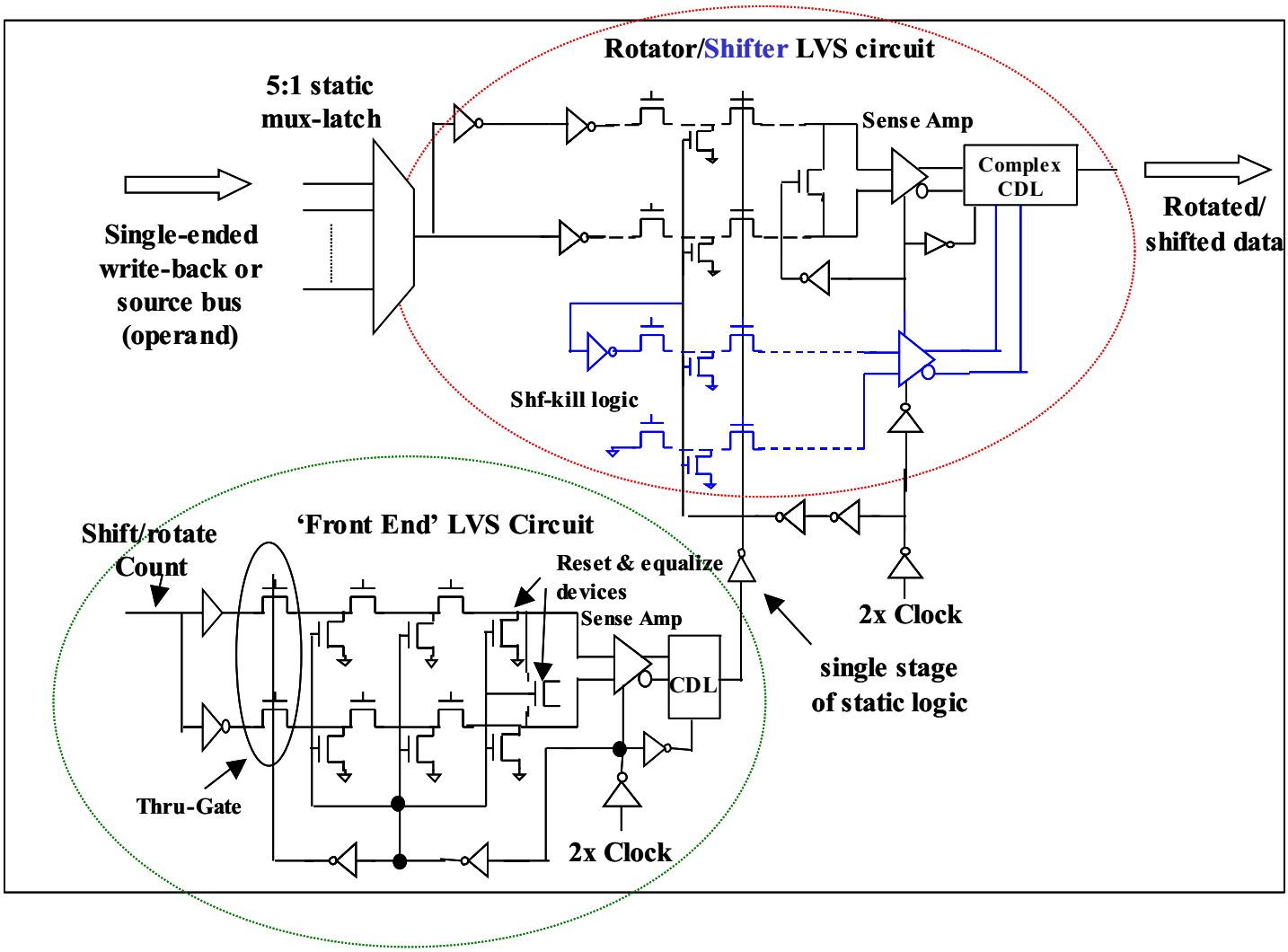

Figure: 8.3.5: LVS rotator/shifter topology.

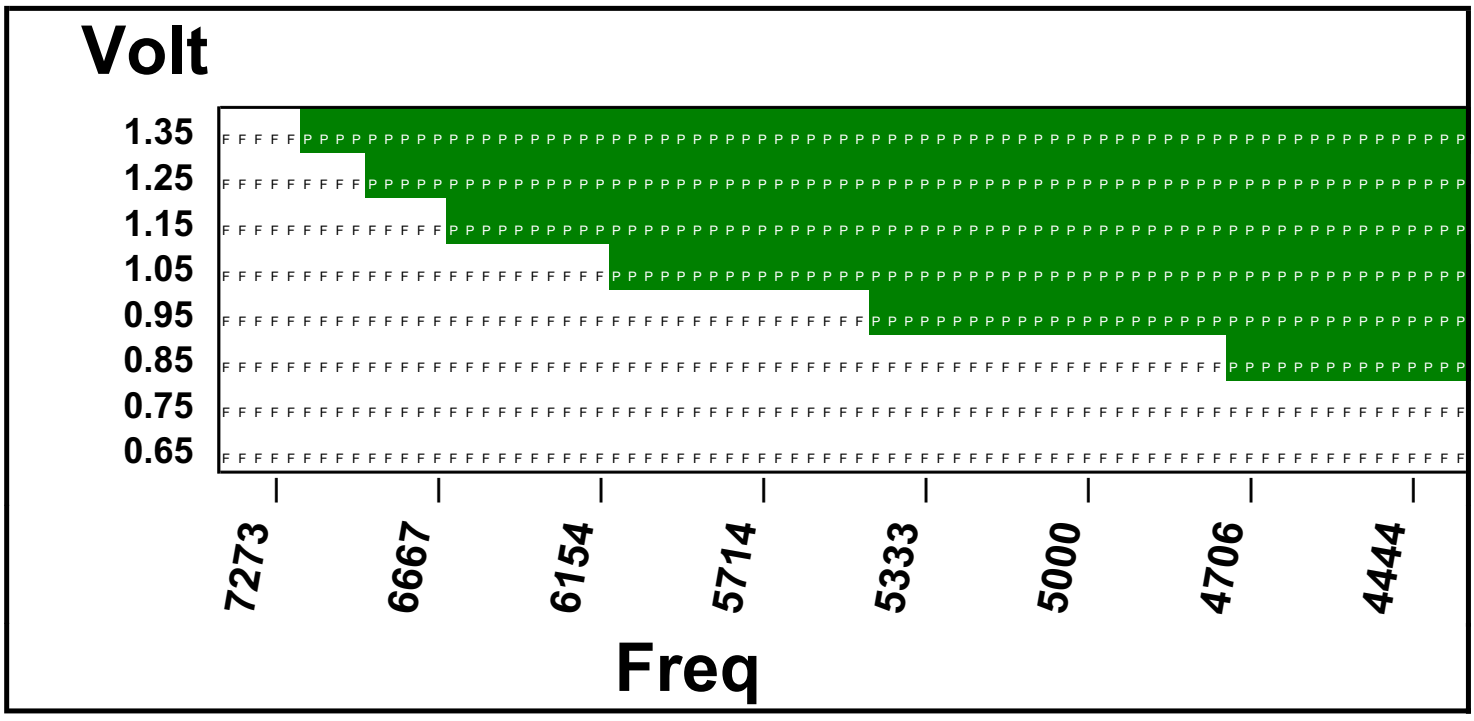

Figure: 8.3.6: LVS 2X clock integer frequency data.

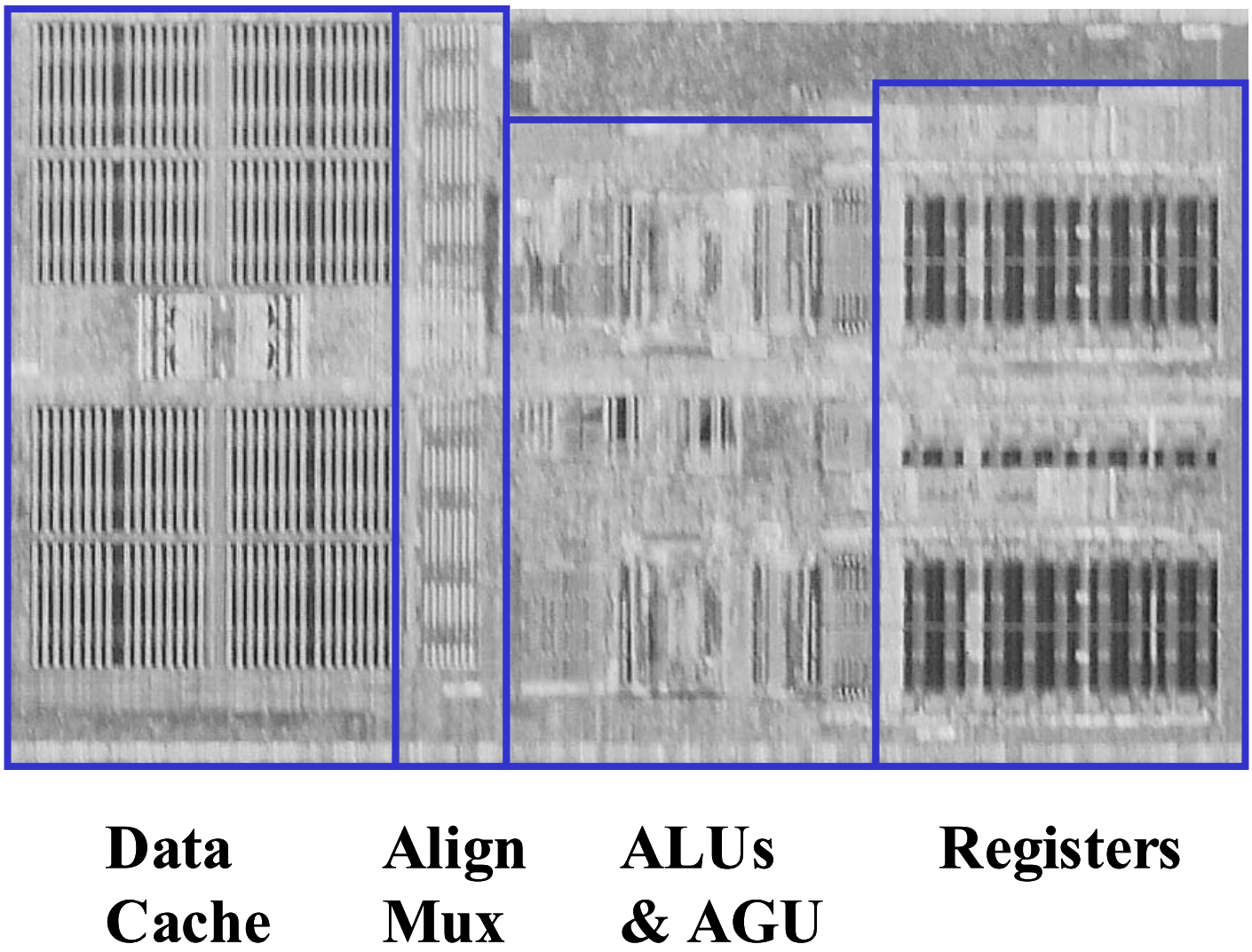

Figure 8.3.7: Integer core micrograph.

0-7803-8267-6/04